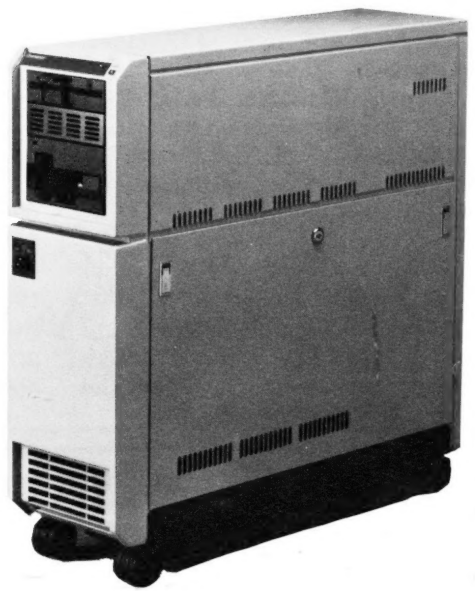
COMPUTER ENGINEERING Section 3

Electronic Engineering Times

Cromemco Coaxes Extra Mips Out Of 2-Mips 68020 μP



The XXU is the engine powering Cromemco's new CS420 line of computer systems.

By R. Colin Johnson

MOUNTAIN VIEW, Calif. — Cromemco Inc. has found a way to squeeze 3 million instructions per second (Mips) worth of performance out of a 2-Mips Motorola 68020 microprocessor.

By adding a 16-kbyte fast (25 ns) static RAM cache on the processor card, Cromemco's new XXU gooses an extra Mips out of the 68020. It also does floating-point operations fast—1.05 million Whetstones per second—by virtue of Motorola's 68881 coprocessor.

Cromemco has been building computers based on the IEEE-696 bus structure since 1974 when it supported only 8-bit data and was called the S-100 bus. Cromemco has prospered over the years by enhancing the bus with first 16-bit and now 32-bit data transfer capabilities as well as incorporating mainframe-like caching strategies. Also, its prowess in high-resolution graphics has landed its systems in over 400 television studios worldwide.

But its XXU 68020 card caps the climax for Cromemco. "No one has tapped the potential of the 68020 like we have, but it didn't come cheap. Cypress Semiconductor's static RAMs are expensive," explained president Harry Garland about the $4,995 price tag on the XXU. The 16 kbytes of cache memory used on the XXU card keeps the 68020 cranking at its full 16.7-MHz speed even if there is a page fault. The proprietary bipolar memory-management unit and Cypress Semiconductor's RAMs still have enough time to refill the cache and get data to the 68020 before its machine cycle ends.

The XXU is also the engine powering Cromemco's new CS420 line of computer systems. As with all Cromemco computers, the 420 line is based on AT&T's Unix System V.2 operating system with virtual memory extensions based on work done at the University of California at Berkeley. This system extends the XXU's caching strategy by adding two lower hierarchical tiers for disks and terminals.

The main processor cache is a two-set associative architecture that virtually assures zero wait state operation.

The disk cache holds in RAM four tracks off the hard disk for fast mass storage transfers. The disk cache can also hold a single track of information being written to disk. This speeds disk write operations as well as allowing for automatic read-after-write verification that the information sent to disk was received properly.

Finally, the terminal cache holds a full screen (2,000 characters) of information for each terminal connected to the 420 system. The 420 can support up to 64 simultaneous users.

A 420 can support up to 16 Mbytes of RAM and 280 Mbytes of internal hard disk storage. A 2-Mbyte system with 140 Mbytes of mass storage goes for $27,995.